CPRE 4920 Status Report 06

3/26/2026 – 04/9/2026

Group number: SDMay26-24

Project title: Digital ASIC Fabrication

Client &/Advisor: Dr. Henry Duwe

Team Members/Role:

Colin McGann	***-Project Lead***
Samuel Forde	***-PCB & Layout Lead***
Michael Drobot	***-Firmware Lead***
Jack Tonn	***-Testbench and Validation Lead***
Dawud Benedict	***-Cache Lead***
Emil Kosic	***-Repository and Coding Standards Lead***
Joshua Arceo	***-Client/Advisor Communications Lead***

- **Weekly Summary**

  Since the last status update, we have integrated the major functional components and started firmware.

- **Past Week Accomplishments**

  - Colin McGann: spi mem 2lc fixes, rasterizer normal, more integration, arbiter simulation timeout, dummy pk slave
  - Jack Tonn: Made address coalescer and the wonderful core block diagram
  - Dawud Benedict: Got core controller to harden, multiple modules down. Fixed cache stuff and got it ready for FPGA testing and integration.
  - Michael Drobot: Integrated WB/PK bridge and fragment FIFO, finally got full pipeline working
  - Sam Forde: Finished spi_mem.v fixes, worked on a script to dump obj files and textures to binary text for testing purposes
  - Josh Arceo: Finished serializer and fragment fifo to serializer. Assisted with integration and worked out bugs found during integration process.
  - Emil Kosic: Continued to work through bugs in integration, successfully cleared the frame buffer with the bridge in simulation

- **Pending Issues**
    - Floorplanning
- **Individual contributions**

NAME	Individual Contributions	Hours this period	HOURS cumulative
Colin McGann	spi mem 2lc fixes, rasterizer normal, more integration, arbiter simulation timeout, dummy pk slave	55	455
Jack Tonn	Core block diagram and coalescer	40	335
Dawud Benedict	Fixed cache, hardened core controller, documentation	25	193
Michael Drobot	WB/PK bridge and frag FIFO integration	25	417
Sam Forde	Spi_mem wrap-up, obj and texture dump script	16	157
Josh Arceo	Fragment Fifo + Serializer, fixed bugs found during integration	15	175
Emil Kosic	Fixed bugs and assisted with bridge integration	20	181

- **Plans for the upcoming weeks**
    - Colin McGann: Integration, fpga and bugfixes
    - Jack Tonn: Document for coalescer and revisit testing section
    - Dawud Benedict: Cache FPGA test, Hardening and help floorplan
    - Michael Drobot: FPGA test and debugging, finishing off RTL integration (cache and bugfixes). Pushing people onto firmware.
    - Sam Forde: Finish the obj and texture dump script
    - Josh Arceo: Write documentation for fragment fifo + serializer, take up a firmware component.
    - Emil Kosic: Continue to work through bridge integration and document the module.